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Harmonic Analysis of Symmetrical and Asymmetrical Cascaded H-Bridge Multilevel Inverter

[a] Muhammad Ammar*, [a] Abdul Sattar Larik, [a] Mukhtiar Ahmed Mahar,[a] Amir Mahmood Soomro,
[b] Muhammad Maaz Siddiqui, [c] Syed Muhammad Sabih Masood
a: Department of Electrical Engineering, MUET Jamshoro.
b: Department of Electrical, University of Windsor Canada.
c: Department of Electrical Engineering, NEDUET Karachi.

***Abstract*—This paper proposes harmonic comparison between symmetrical and asymmetrical CHB MLI using multiple carrier based phase disposition PWM technique (PDPWM). Topologies of different multilevel inverter are reported in the literature, but mainly this work focuses on the harmonic comparison of symmetrical and asymmetrical cascaded MLI with same count of sources and switches. In this paper, PWM switching technique for harmonic comparison of both symmetrical and asymmetrical cascaded MLI is PD. Total harmonic distortion is analyzed in FFT window. Results are observed in SIMULINK/MATLAB software. In these comparative results we can see that an asymmetrical configuration is producing higher voltage levels in voltage output with equal quantity of component compared with the 5-level symmetric inverter and this could lead towards the reduction in harmonic content of output voltage. The benefits of this method of control are applicability and simplicity for n-levels MLI, with no any considerable change in the control circuitry. The experimental measurement results validate proper operation of the discussed MLI.**

***Keywords*- Multilevel Inverter, Cascaded H-Bridge, Phase Disposition, Pulse width Modulation.**

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I. INTRODUCTION

THE Multilevel inverters have drawn growing interest in latest years, in particular within the distributed electrical resources region, because fuel cells, solar cells, rectified wind turbines and several batteries can be connected via a multilevel inverter to feed a load or interconnected to the AC grid without voltage balancing issues.

The Cascaded multilevel inverter is one of several multilevel configurations. The idea of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal output voltage. The voltage output is sum of the voltages which are generated by each cell. The switching angles are needed to be selected in such a way that the THD can be minimized. The generated harmonics certainly cause reduction in the power quality of the whole system. Hence, it is equally important to reduce the harmonic injections from these converters.

Efforts are being made to improve the design of inverters in such a way that not only their power consumption is reduced but also their harmonic contents get minimized.

An N-level CHB Multilevel inverters need 2(n-1) switching devices where the number of output voltage levels are N.

For this purpose, many topologies of inverters have been proposed that give a multilevel output which is near to a complete sinusoidal waveform. The power quality of an inverter output is proportional to the number of levels in output waveform.

Based on the choice of direct current voltage sources used, multilevel inverters are classified as;

1. Symmetrical Multilevel Inverters
2. Asymmetrical Multilevel Inverters

In symmetrical MLI, all of the direct current voltage sources have same voltage amplitude and the output of such inverters is simply the addition of voltages of all direct current sources. By this, the counts of direct current source are equal to the desired number of output voltage levels [2].

While in asymmetric multilevel inverters unequal direct current sources are used to provide more flexibility and increased output voltage levels with the same number of DC sources. Hence, increased voltage output levels can be obtained with the same number of direct current sources. This proves to be a more efficient way for generation of voltage levels [2].

II. METHODOLOGY

The asymmetrical and symmetrical CHB topologies has been modeled to be compared through literature review of easy understanding for best chosen multilevel inverter. Development of simulation model of proposed symmetric and asymmetric inverters using MATLAB/Simulink software. Analysis and Comparison of Harmonics and THD of Symmetric and Asymmetric multilevel inverters using simulation models.

III. SYMMETRICAL CHB MULTILEVEL INVERTER

The configuration of proposed Symmetrical Cascaded H-Bridge MLI is shown in Fig. 1. The Basic switching units can be connected in series to increase the number of voltage level appears in the converter output.

while calculation of size of direct current voltage source for a MLI, it must be noted that all of the voltage steps should be generated in the converter output using available voltage sources.

The proposed inverter can have symmetric configuration such that each one of the direct current voltage source has same values. On this condition, with n number switching units, the number of output voltage steps are equals to

Comparison Between Multilevel Converters		
	Symmetrical Converters	Asymmetrical Converters Binary
N	2N+1	2^{N+1}-1
Sources Number (DC)	N	N
Number Of Switches	4N	4N

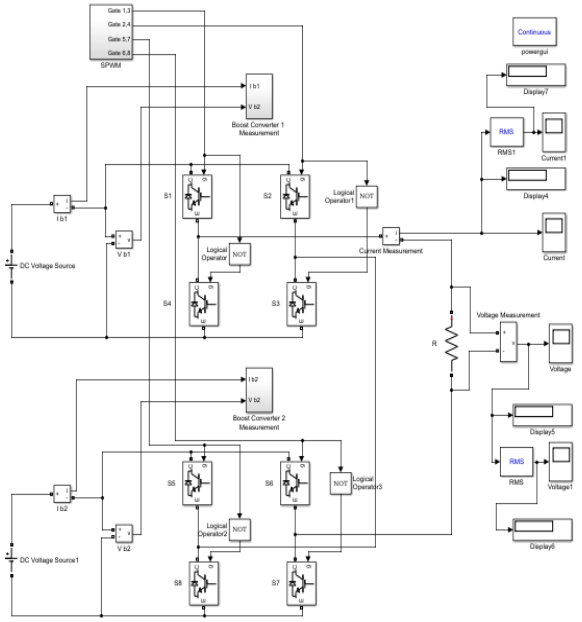


Fig.1
Modeling of Symmetrical Cascaded H-Bridge Multilevel Inverter

Table-I shows switching table of symmetrical CHB MLI with output voltage levels in conventional arrangements as based on different switching states we can get different output voltage levels.

	Switching Table Of Symmetrical CHB MLI								
Mode	Output Voltage	S1	S2	S3	S4	S5	S6	S7	S8
1	+2Vdc	1	1	0	0	0	0	1	1
2	+Vdc	1	1	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0
4	-Vdc	0	0	1	1	0	0	0	0
5	-2Vdc	0	0	1	1	1	1	0	0

Table. I. Symmetrical CHB MLI Switching Table

IV. ASYMMETRICAL CHB MULTILEVEL INVERTER

In symmetrical MLI, all voltage sources have the equal amplitude. That is why the multilevel inverter voltage output is generated by straight adding V_{dc} sources. This is an ineffective methodology for selecting and using direct current sources in the multilevel inverter.

From the other side, asymmetrical multilevel inverter configuration is more efficient way to use proper DC sources. When using of unequal direct current sources V_{dcn} instead of equal sources in asymmetrical configuration. it will give us more variety by changing different values of V_{dc} sources to each other. That is why it generates increased voltage output levels as compared to symmetrical way in similar multilevel inverter configurations. [5]

To select the values of direct current sources V_{dcn} in asymmetric multilevel inverter is a difficult task. Correct values of direct current sources will provide symmetrical and uniformed voltage output levels. Tertiary and binary methods are two common topologies to find out the amplitudes of V_{dcn} in asymmetric configurations.

For trinary method, the amplitude of V_{dcn} is to be selected as a geometric progression of power ‘3’. While in binary, the amplitude of V_{dcn} is to be chosen as a geometric progression of power ’2’.

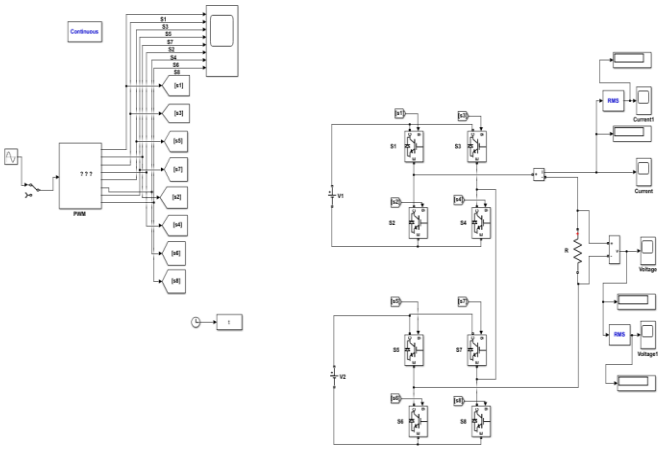


Fig.2
Modeling of Asymmetrical Cascaded H-Bridge Multilevel Inverter

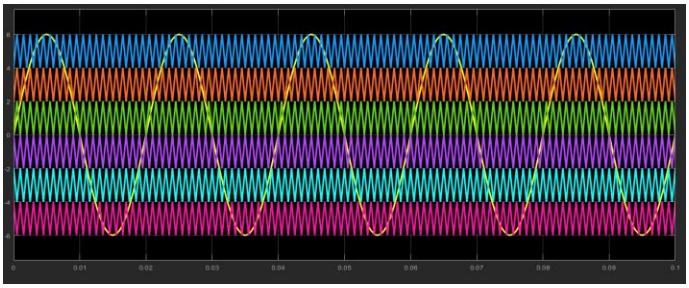
Table-II show switching table of asymmetrical CHB MLI with concerned output voltage levels in conventional arrangements as based on different switching states we can get different output voltage levels.

	Switching Table Of ASymmetrical CHB MLI									
	s1	s2	s3	s4	s5	s6	s7	s8	Vo	
1	1	0	0	1	1	0	1	0	V	V1
2	0	1	0	1	0	1	1	0	2V	V2
3	1	0	0	1	0	1	1	0	3V	V1+V2
4	0	1	0	1	1	0	1	0		0
5	0	1	1	0	1	0	1	0	-V	-V1
6	0	1	0	1	1	0	0	1	-2V	-V2
7	0	1	1	0	1	0	0	1	-3V	-(V1+V2)

Table. II. Asymmetrical CHB MLI Switching Table

V. MODULATION TECHNIQUE

According to the frequencies of switching for multilevel inverters, there are two major groups which can be classified as higher and fundamental switching frequency. [22]. MCPWM method is introduced to achieve an improved quality waveforms of output voltages. Many of the industries implements sinusoidal pulse width modulation technique SPWM for generating switching pulses which is the easiest method. We have used the method in which PWM signals are generated by comparing triangular carrier signals with sinusoidal reference signals. Strategy of phase disposition is applied for the carrier arrangements which have the same frequency, peak to peak amplitude and in phase accordingly. This technique is feasible for reducing the percentage total harmonics distortion(%THD) and distortion factor (DF).



i

Fig. i3

In Fig. 3 which shows the carrier arrangements of sinusoidal pulse width modulation technique with phase disposition strategy to produce output voltage of Asymmetric sequence CHBMLI. From Fig.3, Six carriers are required for producing 7-levels voltage outputs, in which carriers are equally arranged below and above the point zero reference. The triangular carriers continuously compared with sinusoidal reference signal.

VI. SIMULATION RESULTS

The CHB asymmetrical and symmetrical MLI are tested with experimental setup and simulation. Both inverters have equal number of DC sources and switches.

In results we can see that with exact same count of direct current sources we are getting higher level of outputs in asymmetrical inverter.

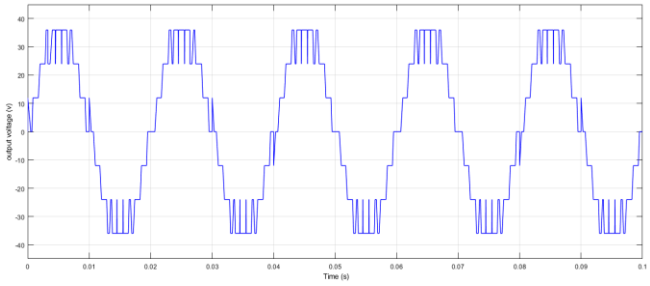


Fig. i4
Output voltage waveform of asymmetrical CHB

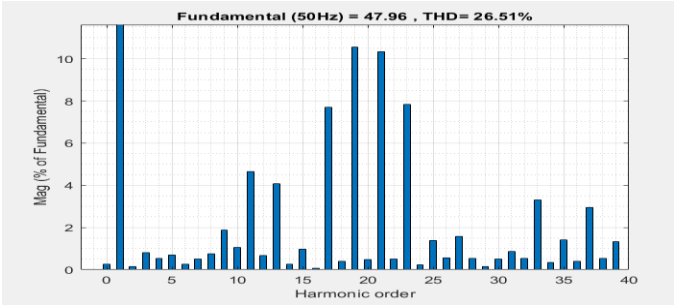


Fig. i5
Harmonic Order of Asymmetrical CHB

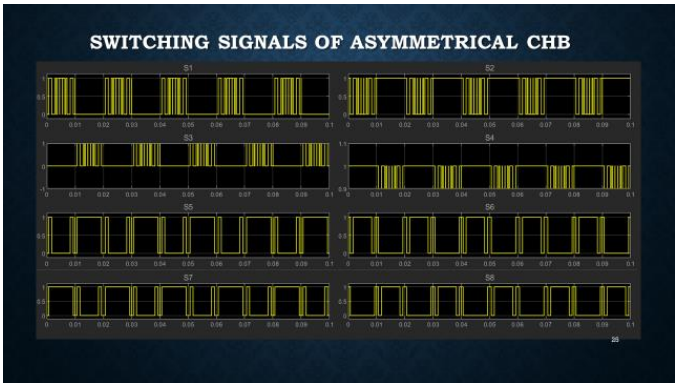


Fig. i6
Switching Signals of Asymmetrical CHB

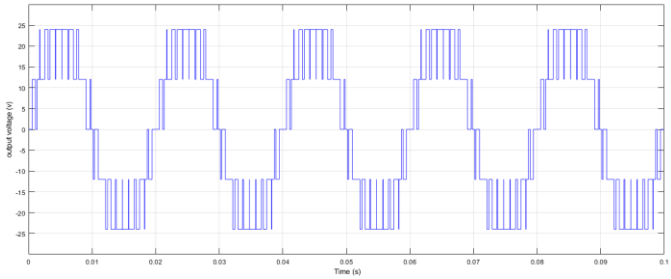


Fig. i7
Output voltage waveform of Symmetrical CHB

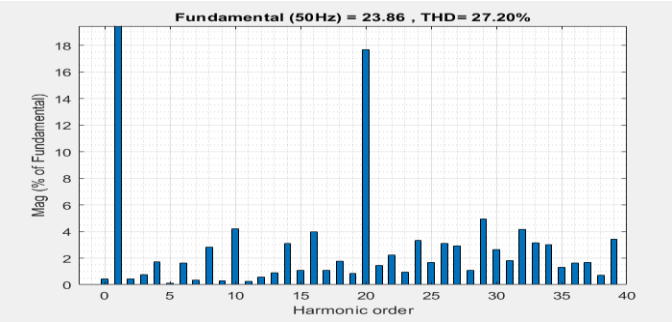


Fig. 8
Harmonic Order of Symmetrical CHB

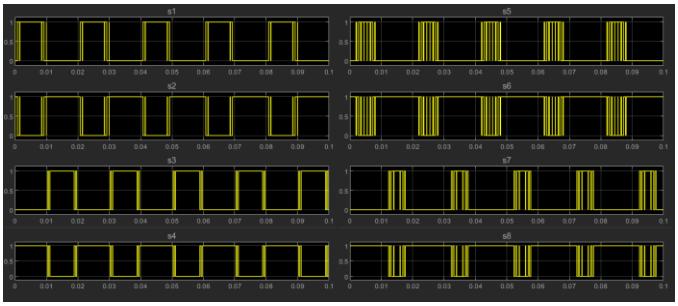


Fig. 9
Switching Signals of Asymmetrical CHB

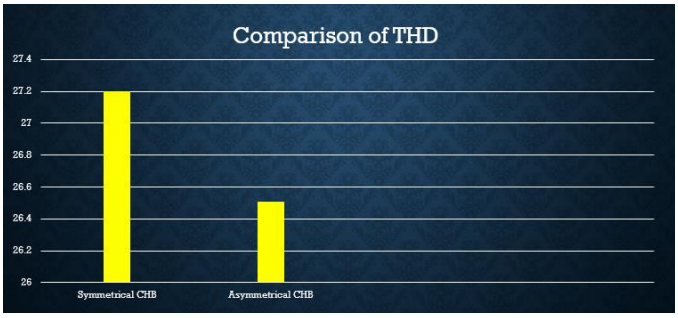


Fig. 10
Comparative THD Results of Both Inverters

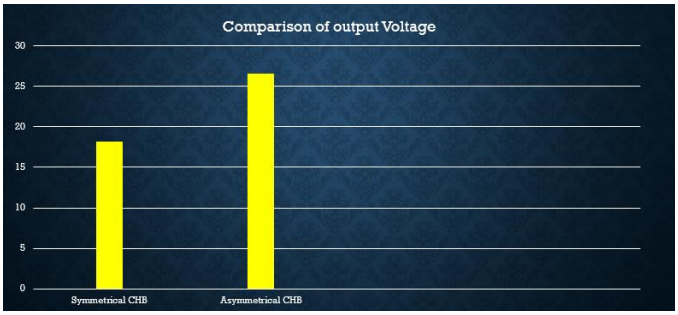


Fig. 11
Comparative Output Voltage Results of Both Inverters

VII. ACKNOWLEDGEMENT

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VIII. CONCLUSION

In this research work, symmetrical and asymmetrical CHB MLIs have been studied.

The simulation models of Symmetrical and Asymmetrical CHB MLI are developed in MATLAB software. The phase disposition MCPWM technique is used to generate the output voltage levels of both converters. The total harmonic distortion in Symmetrical CHB is 27.20 and THD of Asymmetrical is 26.51. From the results, we can be confirming that the Asymmetrical Cascaded H-bridge has less harmonics compared to Symmetrical CHB with same number of switches and sources. Simulation results also show that the Asymmetrical MLI produce more number of voltage output levels as compared to symmetrical cascaded H-bridge multilevel inverter.

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